AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (original): A method of restoring defective memory cells, comprising:

(a) checking all cells of a memory to determine whether the memory is defective at an operation start time;

(b) storing defect information, obtained as a result of the checking, in a memory controller when the checking of all of the cells of the memory is over; and

(c) replacing defective cells in the memory with spare memory provided in the memory controller when there is a request for access to the defective cells of the memory.

2. (currently amended): The method of claim 1, further comprising generating a request for replacing the memory with a new memory when a number of the defective cells in the memory exceeds a predetermined number of data registers.

3. (currently amended): An apparatus for restoring defective memory cells, comprising:

a memory scan controller, which scans a memory in response to a control signal to determine whether at least one cell of the memory is defective at an operation start time and generates defect information; and

a memory controller, which receives the defect information and converts a requested external address into an internal address for accessing the memory, and replaces said at least one defective cell in the memory with spare memory provided in said memory controller, wherein

spare memory, rather than the defective cell, is accessed by ~~the~~ a system controller when the requested external address corresponds to the defective cell.

4. (currently amended): The apparatus of claim 3, wherein the memory scan controller generates a memory replacement signal when a number of said defective cells in the memory exceeds a predetermined number of data registers.

5. (currently amended): The apparatus of claim 3, wherein the memory controller comprises:

first data registers which store external addresses corresponding to said at least one defective cell in the memory;

comparators which compare each of the external addresses stored in the first data registers with the external address applied by the system controller;

second data registers which are activated depending on a comparison result;

a match detector which detects if an external address that matches the external address applied by the system controller exists among the external addresses stored in the first data registers by referring to the comparison result;

a multiplexer which controls a data path to the second data registers or to the memory depending on a detection result of the match detector; and

a controller which loads the external addresses of said at least one defective cell in the memory into the first data registers by referring to the defect information and replaces said at least one defective cell in the memory with the second data registers, depending on the detection

result of the match detector, so that the second data registers can be accessed instead of the defective cell.

6. (currently amended): The apparatus of claim 5, further comprising a delayer which delays an internal address and a control signal before the internal address and the control signal are applied to the memory and when a request is issued for a defective cell in the memory, so that the defective cell and its corresponding replacement second data register are prevented from competing with each other in regard to memory access.

7. (currently amended): A memory controller for converting an external address applied by a system controller into an internal address necessary to access memory, the memory controller comprising:

first data registers which store external addresses corresponding to at least one defective cell in a memory;

comparators which compare each of the external addresses stored in the first data registers with the external address applied by the system controller;

second data registers which are activated depending on a comparison result;

a match detector which detects if an external address that matches the external address applied by the system controller exists among the external addresses stored in the first data registers by referring to the comparison result;

a multiplexer which controls a data path to the second data registers or to the memory depending on a detection result of the match detector; and

a controller which loads the external addresses of said at least one defective cell in the memory into the first data registers by referring to defect information and replaces said at least one defective cell in the memory with the second data registers, depending on the detection result of the match detector, so that the second data registers can be accessed instead of the defective cell.

8. (currently amended): The memory controller of claim 7 further comprising a delayer which delays an internal address and a control signal before the internal address and the control signal are applied to the memory and when a request is issued for a defective cell in the memory, so that the defective cell and its corresponding replacement second data register are prevented from competing with each other in regard to memory access.

9. (currently amended): The apparatus of claim 7, wherein the number of said second data registers is restricted to 0.1% of a storage capacity of the memory.

10. (original): The apparatus of claim 7, wherein an operation speed of the comparator, the match detector, and the multiplexer is faster than a speed of the controller.

11. (original): The method of claim 1, wherein checking is determined complete by scanning for deactivation of a scan signal.

12. (currently amended): The method of claim 1, wherein the memory controller comprises:

first data registers which store external addresses corresponding to said at least one defective cell in the memory;

comparators which compare each of the external addresses stored in the first data registers with the external address applied by the system controller;

second data registers which are activated depending on a comparison result;

a match detector which detects if an external address that matches the external address applied by the system controller exists among the external addresses stored in the first data registers by referring to the comparison result;

a multiplexer which controls a data path to the second data registers or to the memory depending on a detection result of the match detector; and

a controller which loads the external addresses of said at least one defective cell in the memory into the first data registers by referring to the defect information and replaces said at least one defective cell in the memory with the second data registers, depending on the detection result of the match detector, so that the second data registers can be accessed instead of the defective cell.

13. (currently amended): The method of claim 12, wherein the number of said second data registers is restricted to 0.1% of a storage capacity of the memory.

14. (original): The method of claim 12 wherein an operation speed of the comparator, the match detector, and the multiplexer is faster than an operation speed of the controller.

15. (currently amended): The apparatus of claim 5 wherein the number of said second data registers ~~such that the data registers~~ is restricted to 0.1% of a storage capacity of the memory.

16. (original): The apparatus of claim 5 wherein an operation speed of the comparator, the match detector, and the multiplexer is faster than an operation speed of the controller.

17. (currently amended): The method of claim 1, further comprising delaying an internal address and a control signal before the internal address and the control signal are applied to the memory and when a request is issued for a defective cell in the memory, so that the defective cell and its corresponding replacement second data register are prevented from competing with each other in regard to memory access.

18. (original): A computer-readable medium configured to store a set of instructions for restoring defective memory cells, said instructions comprising:

checking all cells of a memory to determine whether the memory is defective at an operation start time;

storing defect information, obtained as a result of the check, in a memory controller, when a checking of all of the cells of the memory is over; and

replacing defective cells in the memory with spare memory provided in the memory controller when there is a request for access to the defective cells of the memory.

19. (currently amended): The computer-readable medium according to claim 18, further comprising: generating a request for replacing the memory with a new memory when a number of the defective cells in the memory exceeds a number of data registers.

20. (original): The computer-readable medium according to claim 18, wherein completion of the checking is determined by scanning for deactivation of a scan signal.

21. (currently amended): The computer-readable medium according to claim 18, wherein said set of instructions further comprises:

storing external addresses in first data registers corresponding to said at least one defective cell in a memory;

comparing each of the external addresses stored in the first data registers with the external address applied by the system controller;

activating ~~said~~ second data registers depending on a comparison result;

detecting if an external address that matches the external address applied by the system controller exists among the external addresses stored in the first data registers by referring to the comparison result;

controlling a data path to the second data registers or to the memory depending on a detection result of the match detector; and

loading the external addresses of said at least one defective cell in the memory into the first data registers by referring to the defect information and ~~replaces~~ replacing said at least one defective cell in the memory with the second data registers, depending on the detection result of the match detector, so that the data registers can be accessed instead of the defective cell.

22. (currently amended): The computer-readable medium of claim 21, wherein the number of said second data registers is restricted to 0.1% of a storage capacity of the memory.

23. (original): The computer-readable medium of claim 21, wherein the comparing, detecting, and controlling instructions operate with a speed faster than the loading instruction.

24. (currently amended): The computer-readable medium of claim 21, wherein said set of instructions further comprises:

delaying an internal address and a control signal before the internal address and the control signal are applied to the memory and when a request is issued for a defective cell in the memory, so that the defective cell and its corresponding second replacement data register are prevented from competing with each other in regard to memory access.